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WHAT IS CLAIMED IS:

1. A method of performing a two stage anneal in the formation of a conductive line, the method comprising:

forming a trench in a dielectric layer;

4 providing a seed layer in the trench;

5 providing a copper material in the trench;

slowly annealing the copper material at a low temperature for

7 a long period of time; and

9

subsequently annealing at a higher temperature than the low

temperature and for a shorter period of time than the long period of time

the copper material to distribute at least one alloy element.

- 1 2. The method of claim 1, further comprising providing a barrier layer along lateral side walls of the trench, the barrier layer being disposed between the seed layer and the dielectric layer.
- The method of claim 1, where in the barrier layer is tantalum (Ta), titanium nitride (TiN), titanium silicon nitride (TiSiN) or tungsten nitride (WNx).
- The method of claim 1, wherein low temperature is less than 100°C.
- 5. The method of claim 4, wherein the long period of time is between approximately 8 and 24 hours.
- 1 6. The method of claim 1, wherein the higher temperature is in 2 a range from 250°C to 350°C.
- 7. The method of claim 1, wherein the low temperature is 80°C or less.

- 8. A method of forming a copper structure in an integrated circuit fabrication process, the method comprising:

 providing a copper seed layer;
 electroplating the seed layer to provide copper material;
 providing a first anneal to form large grain sizes in the copper material; and

 providing a second anneal to distribute alloy elements
- 9. The method of claim 8, wherein the first anneal causes grain growth in the copper material.
- 1 10. The method of claim 8, wherein the second anneal is 2 performed at a higher temperature than the first anneal.

uniformly in the copper material.

- 1 11. The method of claim 8, wherein the alloy elements include at least one of tin (Sn), calcium (Ca), chromium (Cr), zinc (Zn), zirconium (Zr), hafnium (Hf), and lanthanum (La).
- 1 12. The method of claim 8, further comprising:
 2 providing the alloy elements in a layer above the copper
 3 material.
- 13. The method of claim 8, wherein the alloy elements are included in the seed layer.
- 1 14. The method of claim 13, further comprising providing additional alloy elements in a layer above the copper material.
- 1 15. The method of claim 8, wherein first anneal occurs at a temperature less than 100°C.

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- 1 16. A method of forming a damascene conductive structure in an integrated circuit, the method comprising:
- 3 providing a copper layer;
- 4 providing a source of at least one alloy element;
- first annealing the copper layer to cause large grain growth
- 6 over a long period of time; and
- second annealing the copper layer to distribute the at least
- 8 one alloy element in the copper layer.
- 1 17. The method of claim 16, wherein the first annealing occurs
- at temperatures of less than 100°C for more than 8 hours.
- 1 18. The method of claim 16, wherein the second annealing is
- 2 performed after the first annealing.
- 1 19. The method of claim 17, wherein the second annealing is
- performed at temperatures over 250°C and for a time of less than 1 hour.
- 1 20. The method of claim 15, wherein the alloy elements include
- at least one of zirconium (Zr), hafnium (Hf), and lanthanum (La).